OnyX
10G MAC

Overview

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10 Gigabit MAC compliant with IEEE 802.3ae specifications, designed to meet both LAN and WAN requirements. Supports IEEE 802.3x flow-control automatically.

OnyX is targeted at switching applications, avoiding the overhead required for NIC support such as address lists for filtering. For full flexibility and to support multiple instantiations, OnyX is designed for use with external registers and statistics counters.

OnyX interfaces easily to FIFO or Buffer-based system-side data paths, and to either on-chip PCS cores, or vendor-specific DDR i/o cores to provide XGMII interfaces at the link side.

Core characteristics

- *No special cells – light buffering via register arrays*
- *Architected to synthesise easily into ASIC or FPGA implementations – designed for minimum number of logic layers (e.g. pipelined CRC)*

Test suite

- *Comprehensive self-checking Verilog testbench and test suite*
- *Verifies compliance to IEEE802.3ae specifications*

Specifications

- 10 Gigabit MAC compliant with IEEE 802.3ae specifications.
- Compliant with IEEE 802.3x flow-control, handled automatically within the MAC. Option to select externally-generated flow-control frames.
- Supports both LAN and WAN applications, the latter with the aid of an IPG-stretching function.
- Programmable in-band preamble pattern for use in non-standard extensions, such as channelising proprietary chip to chip 10G links, e.g. as an alternative to SPI4.2
- Programmable payload start point (for CRC calculations) facilitates in-band proprietary preamble of any length from 1 to 1k bytes; CRC can be selected to cover or exclude preamble.
- 8-byte wide XGMII equivalent bus designed to interface easily to either on-chip 64-bit PCS, or to vendor-specific DDR i/o macros to operates as a 100% conformant 4-byte XGMII interface.
- Programmable “average IPG” from 8 to 1k bytes on transmit (12 for standard applications); receiver operates with IPG from 5 bytes upwards. Deficit count logic ensures correct aggregate IPG.
- Full-speed CRC-32 calculation at 156.25 MHz
- CRC calculation and appending on transmit can be enabled dynamically – e.g. disabled for switched packets, enabled for routed packets. CRC checked on transmit if contained in packets.
- Jumbo frames supported – max frame size 64kbytes. Programmable max TX and max RX frame sizes : frames truncated above these values if truncation is enabled.
- Received packets under 9 bytes are discarded and flagged; all others (including received flow control frames) passed through to system side and described with a status word.
- Low latency design – no internal FIFOs, light data-alignment buffering only.
- All Status flags needed to support RMON Etherstats group provided for use with external stats counters
- Programmable Big or Little Endian options on Rx and Tx system interfaces.
- Programmable max TX and max RX frame sizes : frames can be truncated above these values.
- WAN mode to achieve an aggregate data rate of 9.58464 Gbps when required, instead of 10.0 Gbps.
- Flexible clock domain options for register interfaces