Pearl

XGS 10G PCS

Overview

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10 Gigabit PCS core compliant with IEEE 802.3ae Clause 48 specifications for PCS

Pearl is targeted at switching applications. For full flexibility, Pearl is designed for use with external registers.

Pearl interfaces to a 10G Mac such as OnyX at the system side, using a single-edge clocked 64-bit 156.25MHz interface, equivalent to a 4-byte 32-bit XGMII 312.5 MHz interface.

Pearl interfaces to 20-bit Serdes cores at the PMA side.

Core characteristics

- *Clock frequency 156.25 MHz (no need for 312.5 MHz)*
- *No special cells – light buffering via register arrays*
- *Architected to synthesise easily into ASIC or FPGAs – designed for minimum number of logic layers, where necessary introducing pipelining to achieve this*

Test suite

- *Comprehensive self-checking Verilog testbench and test suite*
- *Verifies compliance to IEEE802.3ae Clause 48 specifications*

Specifications

- 10GBase-X PCS compliant with IEEE 802.3ae D5.0 May 1 2002 Clause 48 specifications, including all state-machines. This includes :
  - 8b/10b encoding on transmit for each lane
  - 10b/8b decoding on receive for each lane
  - Internal and external framing options for per-lane code-group alignment
  - Lane to lane alignment via per-lane FIFOs, providing a minimum of 16ns skew tolerance
- Bit error test support : IEEE 802.3ae Annex 48A.1, 48A.2 and 48A.3 supported for high and low frequency random jitter testing, deterministic jitter testing, and PLL tracking errors.
- Core clock frequency is 156.25MHz : no need for 312.5 MHz clocks, as functions such as 8b/10b blocks are replicated to handle a double-width bus, to facilitate the lower frequency
- Interfaces to a 64-bit equivalent of XGMII at the system side. This is equivalent to a 32-bit XGMII interface having removed the DDR function, i.e. operates as a true 4-byte interface
- Parallel equivalent of MDIO register interface (not serial) for easier integration into switching ASICs
- Inter-operates with OnyX and other 10G Macs with 64-bit XGMII equivalent interfaces, in standard IEEE 802.3ae mode. Also interoperates with OnyX in it's non-standard modes of operation, such as non-standard IPG, preamble patterns and payload offsets
- IPG is maintained through PCS with no idle insertions or deletions. Receive path remains in receive clock domain (not transferred to ASIC system clock domain), avoiding the need for idle insertions/deletions to handle clock domain crossing.
- Comprehensive check features, including visibility bus and latching of transitory conditions (all brought through to ASIC clock domain).
- Flexible configuration options, such as depth of Align FIFOs, maximum skew and external control of synchronisation and deskew processes.