AXI3, AXI4, AXI4-Lite Interconnect UVM based Verification IP

Revision	Initials	Date	Description
1.0	SMG, GL	15th August 2016	Summary datasheet - initial revision

1 Introduction

This document describes the functionality of a UVM based AXI3, AXI4, AXI4-Lite Interconnect Verification IP.

The VIP provides a test environment to fully test the functionality of an interconnect connecting any combination of AXI3, AXI4, or AXI4 Lite Masters and Slaves.

The VIP is designed to stress test any interconnect to quickly identify and debug any issues or bugs present in the DUT.

The UVM testbench environment is shown in Figure 1.1 and described in further detail below.

Parameters specific to the DUT (AXI Interconnect) can be randomly constrained in each test run and then passed to the main testbench.

2 UVM Testbench Components

- ***axi_top***

  The top level of the VIP. The DUT (Interconnect), all interfaces and UVM environment are instantiated here.

- ***axi_env***

  Master/Slave agents and scoreboard are instantiated here.

- ***env_config_db***

  Used to configure environment specific parameters, such as number of masters, number of slaves, master type, slave type will be constrain randomly defined here.

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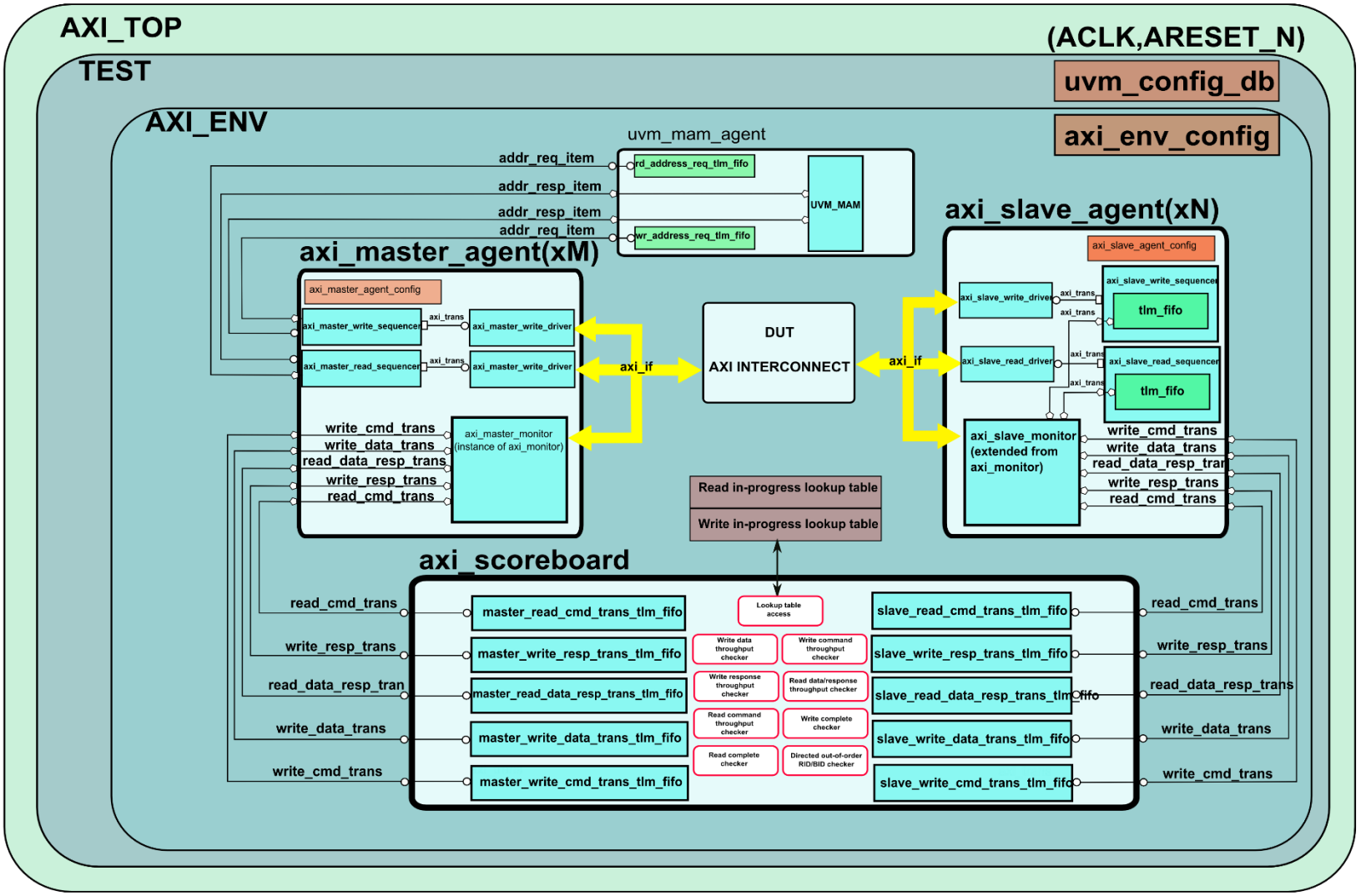

Figure 1.1 – UVM testbech environment for testing AXI Interconnect

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➢ *axi_master_agent*

Models behavior of either an AXI3, AXI4 or AXI4 Lite Master. Randomly generates and sends AXI read and write transactions. axi_master_sequencer, axi_master_driver and axi_master_montior are instantiated here.

○ axi_master_sequencer

Converts sequences randomly generated from test into transactions which are then sent to the driver.

○ axi_master_driver

Drives AXI signals across the bus based on information from transaction. Randomly generates data on the WDATA line.

○ axi_master_monitor

Observes the AXI interface and passes transaction information to the scoreboard. Sends five different transactions based on each channels information: write_cmd_tx, write_data_tx, write_resp_tx, read_cmd_tx, read_data_resp_tx.

➢ *axi_slave_agent*

Models behavior of either an AXI3, AXI4 or AXI4 Lite Slave. Responds in a random order to one of the write or read transaction requests it received. axi_slave_sequencer, axi_slave_driver and axi_slave_montior are instantiated here.

○ axi_slave_monitor

Observes the AXI interface and passes transaction information to the scoreboard in same way as axi_master_monitor. Additionally, sends an axi_trans object (transaction) to the axi_slave_sequencer to let it know when a read or write transaction has been requested.

○ axi_slave_sequencer

Receives write or read request transactions from the monitor, and responds to them in a random order.

○ axi_slave_driver

Drives AXI signals back across the bus based on information from transaction. Randomly generates data on the RDATA line.

➢ *axi_scoreboard*

Stores transaction information received from all monitors and decides whether the interconnect is performing correctly. Provides debug information to quickly identify error routes and bugs in the design.

- Checks all AXI transactions are completed in correct order and in time (if timeout used).
- Checks all commands and transactions are routed to the correct Slave and Master ports.
- Checks all data and information passing through the DUT remains uncorrupted.
- Checks data transactions match the associated command.
- Checks all transactions are appropriate for the associated Master or Slave types (ie AXI3/AXI4 or AXI4 Lite).

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